All-Optical Packet-Drop Demonstration Using 100-Gb/s Words by Integrating Fiber-Based Components

T. J. Xia, *Member, IEEE,* Y. Liang, K. H. Ahn, *Student Member, IEEE,* J. W. Lou, *Student Member, IEEE,* O. Boyraz, *Student Member, IEEE,* Y.-H. Kao, *Student Member, IEEE,* X. D. Cao, S. Chaikamnerd, J. K. Andersen, *Student Member, IEEE,* and M. N. Islam, *Senior Member, IEEE*

***Abstract*—Packet-drop function for a time-division multiplexing network using 100-Gb/s, 8-b words is experimentally demonstrated by integrating all-optical header processing and payload demultiplexing with electrooptic packet routing. The header processor consists of two levels of all-optical logic gates based on low birefringent nonlinear optical loop mirrors (NOLM's), and the payload demultiplexer is a two-wavelength NOLM. Both devices are driven by synchronized lasers with timing jitter under 1 ps. The contrast ratios for both header processor and demultiplexer are 10:1 and that of the packet router is 17 dB. The switching energies for header processing and payload reading are 10 and 1 pJ/pulse, respectively.**

***Index Terms*— Optical control, optical fiber communication, optical logic devices, optical signal processing, optical switching, packet switching, time-division multiplexing, ultrafast optics.**

ALL-OPTICAL serial processing can be important for high-speed time-division multiplexing (TDM) networks as single-channel speeds exceed electronic capabilities. Although many all-optical devices have been individually demonstrated, there are very few experiments combining these devices to provide network functionality [1]. We experimentally demonstrate the packet-drop functions for an access node of a 100-Gb/s packet TDM network by integrating synchronized short-pulse lasers, all-optical header processor, electrooptic packet router, and payload demultiplexer. This node is designed for a 100-Gb/s soliton ring network [2]. By combining these emerging all-optical technologies, we confront some of the key challenges of 100-Gb/s packet TDM networks, including operation of multiple levels of all-optical logic gates, synchronization between the incoming data and the local source, and power budget for operation of the node. Our demonstration shows the inter-compatibility of the various optical components as well as the network functionality of all-optical header processing and demultiplexing. Using an 8-bit, 100-Gb/s word, we achieve 10:1 contrast ratios from the header processor and the demultiplexer and 17-dB contrast ratio from the packet router.

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The authors are with the Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109 USA.

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Previous subsystem demonstrations have used semiconductor devices and simplified architectures. Cotter *et al.* route 100-Gb/s, 6-bit packets using a single AND-gate as the header processor [3]. To use a single AND-gate to process the header, the header is designed to have special bit patterns, which allow the AND gate to distinguish headers. In addition, Glesk *et al.* demonstrate all-optical address recognition and self-routing in a 250-Gb/s packet-switched network [5], in which a switch operating only 1 bit for each packet is used. Compared to the previous demonstrations, our node architecture enables more general optical serial processing capabilities because of increased flexibility through the possibility of using multiple levels of logic operation. The fiber based NOLM's, which are used as the optical logic gates in this letter, have been shown to have unique properties such as ultrafast speed, cascadability, and Boolean completeness [9]. Even though only two levels of all-optical logic operation have been demonstrated in this letter, further levels of operation are possible because the logic gates are regenerative. Multiple levels of logic operation permit multiple processing on the header, for example, to check empty packets, bit errors, or special conditions. Our previous work demonstrated the header processor function alone [8]–[9]. Here, we demonstrate packet-drop funtion by integrating the transmitter, header processor, packet router and demultiplexer.

A block diagram of the access node is shown in Fig. 1. An 8-bit packet (3-bit header "011," 5-bit payload "10 010") is generated by the transmitter and sent to the node. Upon entering the node, part of its energy is tapped to the header processor, and the rest is passed to the router through a delay line. A local laser (slave laser #1) in the node, which has the same wavelength as that in the transmitter, is synchronized to the transmitter (master laser). The local laser generates clock pulses and local header bit patterns for the all-optical logic inverter and XOR gate. The inverter determines the packet is empty if all bits are "1" in the header. If the packet is not empty, the inverter sends an inverted header pattern to the XOR gate. A local header generator sends either a matched or mismatched inverted header to the XOR gate. If the headers match at the XOR gate, there is no output, and the packet will go to the demultiplexing unit. If the headers do not match, the XOR gate output has at least one "1," which will trigger the control of the packet router to shift the packet

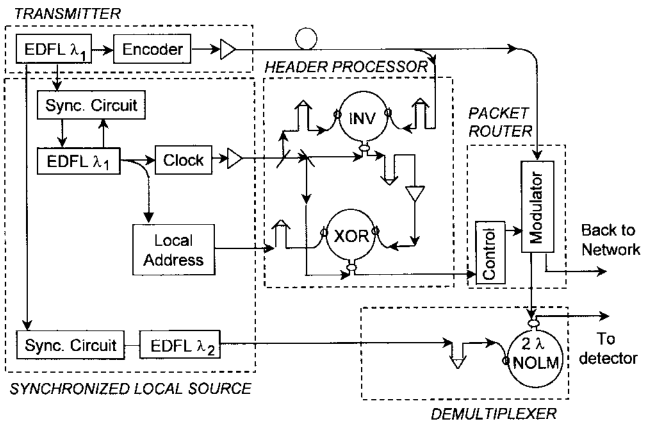

Fig. 1. Detailed diagram for the packet-drop experiment. The transmitter consists of a master laser and a packet encoder. The packet-drop part consists of synchronized local lasers, a local header generator, a clock pulse train generator, a header processor, a packet router, and a demultiplexer. INV—inverter, XOR—exclusive OR gate, 2-λ NOLM—two-wavelength nonlinear optical loop mirror, and EDFL—erbium-doped fiber laser.

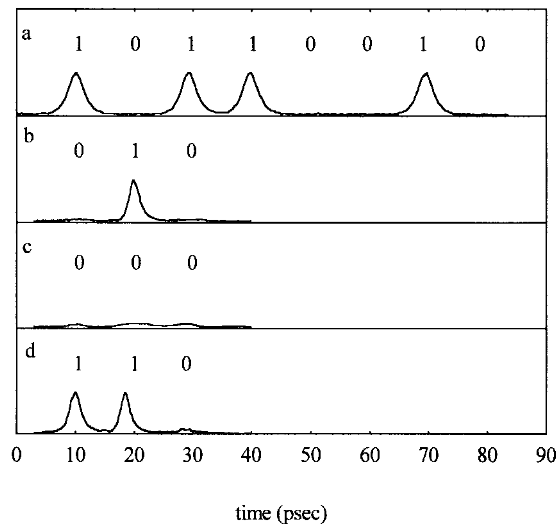

Fig. 2. Cross-correlation results of the header processor. (a) Input data packet; (b) Output of the inverter; (c) Output at the XOR gate when the headers match; and (d) Output at the XOR gate when the headers do not match (the inverted incoming header is 010 and the local header is 100).

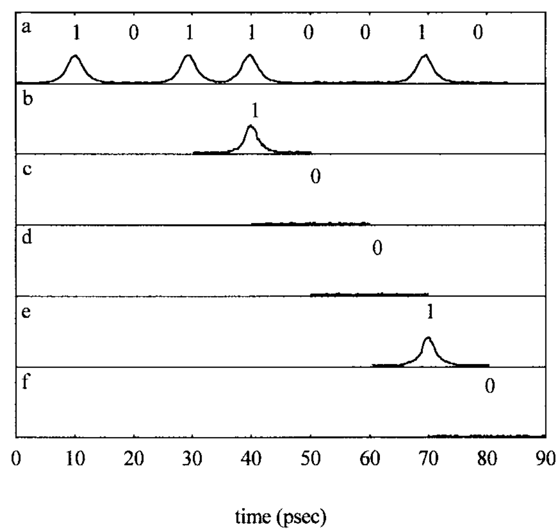

Fig. 3. Autocorrelation results of the demultiplexer. (a) Input data packet; (b)–(f) Output of the 2-λ NOLM by adjusting the delay of the local pulse by an additional 10 ps each time.

back to the network. The payload in the packet going to the demultiplexer is read by a two-wavelength nonlinear optical loop mirror (2-λ NOLM) [4]. The control pulse comes from another synchronized local laser (slave laser #2), which has a wavelength different from that of the transmitter. Each component in the node is described in the following.

The master laser and the slave lasers are passively mode-locked, Er/Yb co-doped fiber lasers [6]. The average output power is 5 mW at 1535 nm for both master laser and slave laser #1, and 1543 nm for slave laser #2. The pulsewidths are 2 ps (FWHM) with a nearly transform-limited hyperbolic secant shape. Synchronization of the master laser and slave lasers is realized by sending a separate clock pulse from the master laser to the slave lasers [7]. This synchronization is designed for correction of slow drifts of the remote clock pulse rate, and the response bandwidth is 10 kHz as restricted by the AOM. Although the laser repetition rate is 21 MHz, 100-Gb/s words are created by splitting each laser pulse and combining them with couplers and delay lines. The local laser pulse is aligned to the first pulse of the packet. Therefore, the clock and local header align the header and payload automatically for fixed header and payload lengths.

The all-optical logic gates are realized by using low birefringent nonlinear optical loop mirrors (low-bi NOLM's). The low birefringence $(\Delta n \approx 3 \times 10^{-6})$ is generated by wrapping fibers with very low background birefringence on aluminum mandrels. This low birefringence allows the co-propagating pulses along orthogonal polarizations in the loop to phase shift through cross-phase modulation (XPM), and insures that two pulses have a reasonably long interaction length, while the high extinction ratio maintains a good output contrast ratio. The walkoff distance is ~115 m and the extinction ratio is ~40:1. One major advantage of this kind of optical logic gates is its cascadability. This logic gate is regenerative, which allows multiple levels of all-optical logic operation. Another advantage is the timing window, which makes the NOLM's tolerant to possible timing jitter between the bits. The logic gates are Boolean complete, with switching energies of 10 pJ/pulse, timing windows of 5 ps, and nonlinear transmissions of 50% [8]–[9].

The demultiplexing and packet routing use guided-wave optical structures. The 2-λ NOLM with a timing window of 6-ps demultiplexes the payload into individual bits. This 2-λ NOLM uses a high nonlinearity, dispersion-shifted fiber ($\lambda_0 = 1530$ nm), which has a smaller core size (effective area $A_{\text{eff}} = 17\ \mu\text{m}^2$) to increase optical intensity and a higher germanium doping to increase the intrinsic nonlinear coefficient. The effective nonlinearity is 4.4 times that of a normal dispersion-shifted fiber. The switching energy of this device is less than 1 pJ/pulse. A commercial 2 × 2 $LiNbO_3$ modulator is used as the packet router.

The header processor output is detailed in Fig. 2. The data packet including the header is given in Fig. 2(a), while the inverted header output from the inverter, which is used as the

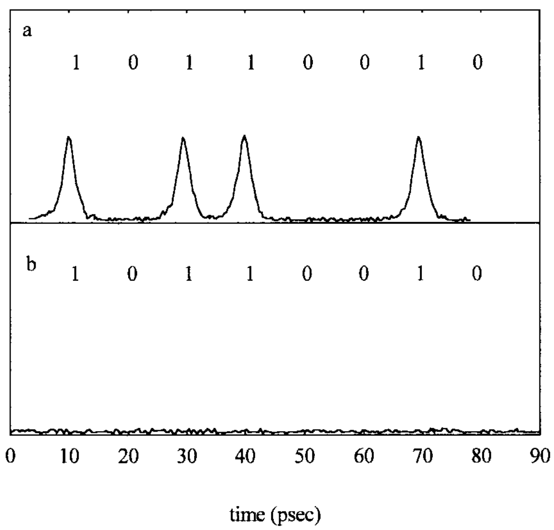

Fig. 4. Cross-correlation results of the output of the packet router. (a) The incoming header does not match the local header (packet sent back to network); (b) The header matches the local header (packet sent to demultiplexer).

input of the second logic gate (XOR), is given in Fig. 2(b). The XOR gate output when the header matches (does not match) the local header is given in Fig. 2(c) [Fig. (2d)]. This output is detected and used to drive the packet router. The on–off contrast ratio after the cascaded gates is 10:1. The contrast ratio is limited by pulse distortion from the erbium-doped fiber amplifiers (EDFA's), which leads to incomplete switching through degradation of the polarization extinction ratio.

The demultiplexed output for each channel is shown in Fig. 3 for the case when the incoming and local headers match. For channels (1–5), the clock pulse is delayed by 10 ps each time to select the appropriate bit. The contrast ratio is 10:1. The residual signals in the "0" bits indicate pump leakage and energy tails from the adjacent "1" bit of the payload. These residual signals are not visible in Fig. 3 because we use an auto-correlation to see each individual bit.

The output returning to the network from the $LiNbO_3$ modulator is illustrated in Fig. 4. When the incoming header does not match the local header, the packet is routed undistorted. The contrast ratio of the signal returning to the network is 17 dB.

These preliminary results show inter-compatibility of the all-optical components toward a packet TDM access node. The major challenges are multiple levels of all-optical logic operation, low jitter synchronization, and power budget. Our results prove that the fiber-based optical logic gates are cascadable and can be used to perform multiple levels of all-optical logic operation. The synchronization scheme used in this letter shows a very low-timing jitter (<1 ps). By using the low birefringence to increase the walkoff distance in the header processor, we have been able to lower the switching energy to about 10 pJ/pulse. The range of switching energies for the header processor is 5–15 pJ/pulse, and that for the demultiplexer is 0.5–1.0 pJ/pulse. If the energy is too low, the output contrast ratio is poor, whereas if the energy is too high, pulse distortion occurs in the loop mirror. Here, the node is designed for one-to-one communication. For broadcast capabilities, a special address can be added to the header and one more level of optical logic operation may be needed. To avoid errors from possible node failure, the packet router switch will be set to direct the data back to network when there is no power to the node.

In summary, all-optical serial processing is used experimentally for the 100-Gb/s packet-drop part of a packet TDM network access node. The two cascaded low-bi-NOLM's have switching energies of 10 pJ/pulse and contrast ratio of 10:1 for the entire header processor, while the demultiplexer has a switching energy of less than 1 pJ/pulse and contrast ratio of 10:1. The packet is routed with a contrast ratio of 17 dB.

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